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# Comparative Analysis of Noise, Power, Delay and Area of Different Full Adders in 45nm Technology

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***Abstract :*** *VLSI Circuit Design is a significant subject for instance like adders and multipliers for the implementation of a various of logic and arithmetic functions likes of basic circuit approach and topology. Full adders like digital signal processors (DSP) architectures and microprocessors are vital elements in the application. Apart from that, the adding of two numbers is main assignment. it's key that determines the overall speed of the critical path lies in the vast majority of these systems like subtraction, multiplication , division , address calculation system as participate in many other activities . So the 1 -bit full adder cells (connective building blocks) is an essential objective of attractive performance. This paper show relative study of high-speed, low-power and low voltage full adder circuits. Our aim is to compare different XOR - XNOR full adder based circuit to and designs a high efficiency adder. We have studied 27 different combinations of adders and studied noise, average power, the ability to delay, utilization of space in 45nm technology.*
***Keywords****: CMOS, XOR-XNOR circuit, SERF, TG, TFA, MUX, and CPL.*

## I. Introduction

A lot of hard work in research in the field of digital electronics in the past year has been focused towards growing speed of digital systems. In recent times, the need for portability of the circuit and the low power supply is the most important parameters to design the efficient VLSI design. Power outages activity and changes in the size of the circuit (gate, diffusion, and wire capacitances formed) is dependent on the node capacitances. Power utilization of a CMOS digital circuit can be represented as

$$P = f\,C\,V_{dd}^{\,2} + f\,I_{short}\,V_{dd} + I_{leak}\,V_{dd} \quad (1)$$

Where f is the clock frequency, $I_{short}$ short circuit current, C is the average switched capacitance per clock cycle, $V_{dd}$ is the supply voltage, and off current is $I_{leak}$ [29]. A well- optimized low power VLSI circuits, 1st term in the equation (1) is dominant so far. Supply voltage scaling is the most efficient way to sink power utilization. On the other hand, a low supply voltage amplifies the circuit delay and logic circuit output push to decrease. A major barrier of decreasing the supply voltage is the transistor count and $V_{th}$ loss. Suitable (W / L) ratio of the power dissipation can be diminishing without reducing the supply voltage.

## II. Circuit Design Style

Power utilization, performance, space captured, noise invulnerability, reliability and good dynamic power in the variety of complication associated with the full adder. Many researchers have suggested the hybrid dynamic static full adders [20] for efficient design. Another study of the low power design is pass-transistor logic which is described in previous research [1]-[4].

Digital computing systems is a basic 1 -bit full adder cell with three inputs (A, B and C) and two 1 -bit outputs (sum and carry). With different logic terminology, this output can be derived. Therefore, a full adder circuit can be designed as follows.

$$SUM = A.B.C + A.\overline{B}.\overline{C} + \overline{A}.B.\overline{C} + \overline{A}.\overline{B}.C = \overline{Carry}(A+B+C) + (A.B.C) \quad (2)$$

$$Carry = A.B.C + A.B.\overline{C} + \overline{A}.B.C + A.\overline{B}.C = AB + C(A+B) = A.B + B.C + C.A \quad (3)$$

XOR logic using the logical Boolean expressions in the input and output logic is demonstrated as:

$$Sum = A \oplus B \oplus C and Carry = AB + (A \otimes B) \quad (4)$$

$$Sum = \overline{C}(A \oplus B) + C(A \otimes B) and Carry = C(A \oplus B) + A(A \otimes B) \quad (5)$$

Exclusive-OR and, Exclusive-NOR, denoted by $\oplus$ and $\otimes$ respectively, the following Boolean functions that perform binary operations –

$$A \oplus B = \overline{A}B + A\overline{B} \quad and \quad A \otimes B = AB + \overline{A}\overline{B} \quad (6)$$

This paper is to be used as the root of contrast, the full-adder cell topology for the execution of principles. Some typical completion is as follows: CMOS logic styles have been used to execute a low-power 1-bit adder cell.

1. Conventional CMOS full adder (CMOS) transistors, comprising 28 regular CMOS structure (pull -up and pull-down network) are depending on.
2. Adder 24 comprises a Mirror Transistor.
3. Complementary Pass Transistor logic (CPL) full adder using 22 transistor and CPL gates.
4. SDCVSL full adder depends on Cascode Voltage Switch Logic (CVSL) the style.
5. Transmission - Gate CMOS adder (TG - CMOS) and the transmission function adder (TFA) depend on transmission gate logic.
6. The new (TG-Pseudo) full adder is depend on transmission gate and pseudo logic.
7. Hybrid full adder 26 having transistors are customized low- power XOR / XNOR circuit.
8. GDI XOR, GDI XNOR gate diffusion input like (GDI) formed on full adder.
9. Multiplexer full adder circuit (MBA 12T) using less energy.
10. Serf, CLRCL, 8T, 9T, 10T, 13T, 14t and 16T low- power full- adder cell. Its low power XOR / XNOR gates based on pass transistor logic design and transmission gates.

All static full adder circuit output can be separated into two groups on the basis of performance. The first set to have full swing output of full adders. C- CMOS, CPL, TG, TFA, Hybrid, 14t and 16T full adders are in the initial set [1]-[8]. Without full swing output, the second set are full adders (10T, 9T & 8T) [9]-[25] , the full adders typically based transistors (4T/3T) less number of XOR / XNOR circuit , low power utilization and possession of the area .

1.1 Mirror Adder

NMOS and PMOS chains are entirely proportioned. A maximum of two series transistors can be observed in carry generation circuitry. When lying out of the house, the most important thing is minimization. Reduction of the diffusion capacitance at node Co is particularly important. The node capacitance Co is composed of four diffusion capacitances, two internal gate capacitances, and six gate Connect adder cell capacitances. C is connected transistors are placed closest to the output. Only carry- stage transistors are optimized for optimal speed. The sum of all of the transistors can be summarized size. Figure.1 shows the circuit diagram of Mirror Adder.

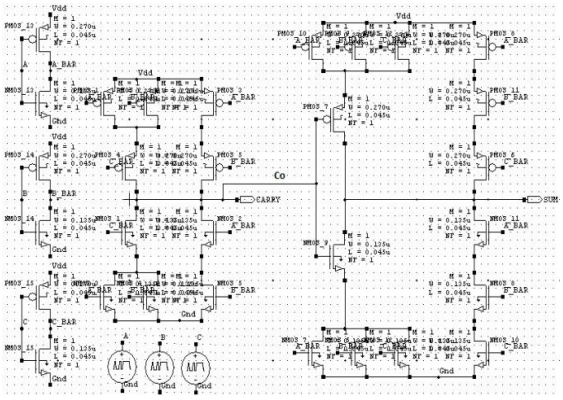


Fig.1. Circuit Diagram of Mirror Adder

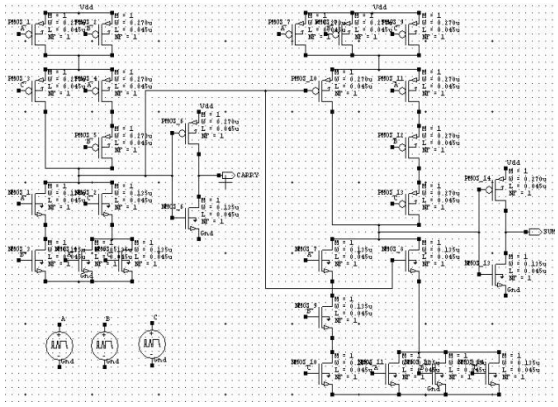


Fig.2.Circuit Diagram of Conventional Full Adder

1.2 Conventional Static CMOS Logic – CSL

Conventional static CMOS logic chip model is shown in Figure.2 and used in the majority of the modern VLSI applications. Each stage of PMOSFET and NMOSFET set-up is dual set of connections. Capacitive load drive current with the purpose of obtain a practical effect of transistor width must be enlarged. This is shown amplified input capacitance and therefore results in higher power dissipation and propagation delay of this. Figure.3 and Figure.4 shows TG Adder and TFA Adder respectively, having full swing outputs.

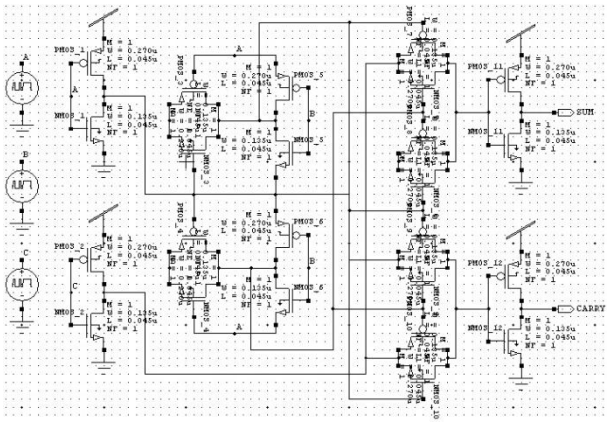

Fig.3. Circuit Diagram of TG Adder

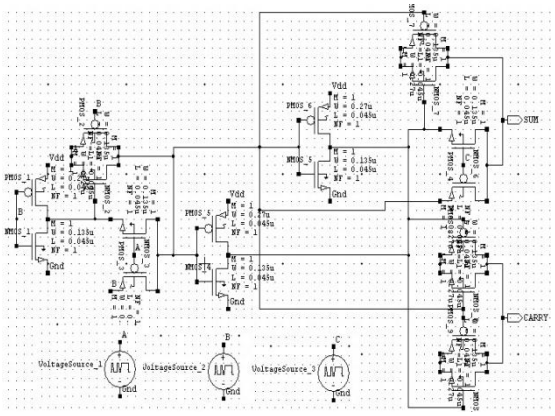

Fig.4. Circuit Diagram of TFA Adder

1.3 Complementary Pass Transistor Logic – CPL

The foremost idea of CPL [23] is to execute logic functions using only a NMOSFET arrangement. As a result, we get low input capacitance and high speed operation. Figure.5 shows the circuit diagram of CPL Adder. Pass - Transistor Output is less than the supply voltage level Due to high voltage level transistor threshold voltage, the output signal will be improved by the application of CMOS inverters. Pass transistor output switching power is dissipated in charging or discharging to be shown

$$P_D = V_{dd}\ V_{swing}\ C_{node}\ F \quad (7)$$

Where $V_{swing} = V_{dd}\ V_{thn}$. PMOSFET's incomplete shut down at the output of inverters to minimize static current, supply voltage level of a weak PMOSFET feedback device can also be supplemented pass - transistor output circuits to full supply voltage level with the intention of pull the CPL.

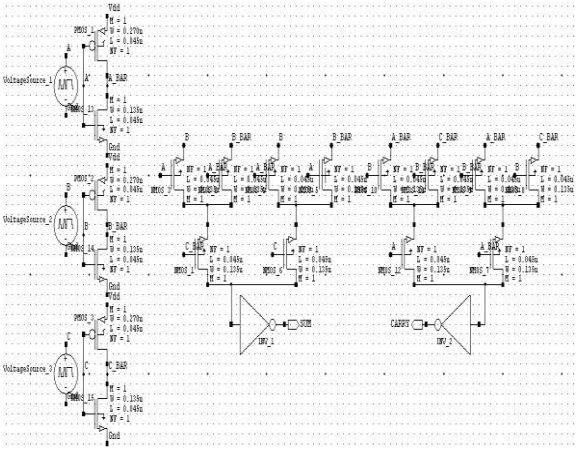

Fig.5.Circuit Diagram of Complementary Pass Transistor Logic

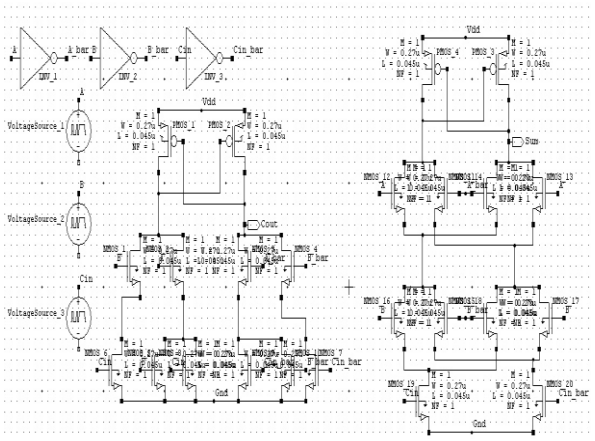

Fig. 6.Circuit Diagram of Static Differential Cascode Voltage Switch Logic – SDCVSL

1.4 Static Differential Cascode Voltage Switch Logic – SDCVSL

Figure.6. shows the circuit diagram of SDCVSL Full adder. By a duo cross- coupled PMOSFET, corresponding NMOSFET transistor switching hierarchy is designed. Derived from the various input, any output is pulled down its NMOSFET system. The cross- coupled PMOSFET transistors have secured and fasten the Differential output. As switching NMOSFET transistors hierarchy is motivated by input, by comparing conventional static CMOS logic, input capacitance is typically two or three times little .

1.5 XOR-XNOR Based Full Adder Topology

Enhancement the output, Hybrid full adder has been intended with Pass logic circuits and transitional XOR-XNOR simultaneously. Hybrid full adder's carry- generator unit is a complementary CMOS logic approach depends on MUX. The most awful case is delay in conversion from 01 to 00 and 10 to11, that's why PMOS and NMOS transistors sequence are adding to solve. Even if alteration of XOR / XNOR circuit get better speed, but these extra transistors enlarge the power utilization of the full adder unit. The hybrid logic is applied one more XOR circuit which is executed by pass transistors for making sum. Output of the inverter recover the

voltage level and get better driving capability for Cascading. At a small voltage, characteristics like full swing logic, reasonable outputs and best output drivability are getting by 26 transistors [16]. Another hybrid full adder is considered with the arrangement of low power transmission gates and Pseudo NMOS gates. Transmission gate made up of a PMOS transistor and an NMOS transistor logic which is an unusual kind of pass-transistor logic connecting in parallel. No voltage drop at the output side is present, but here the number of transistors are double which is needed to intend the equivalent purpose.

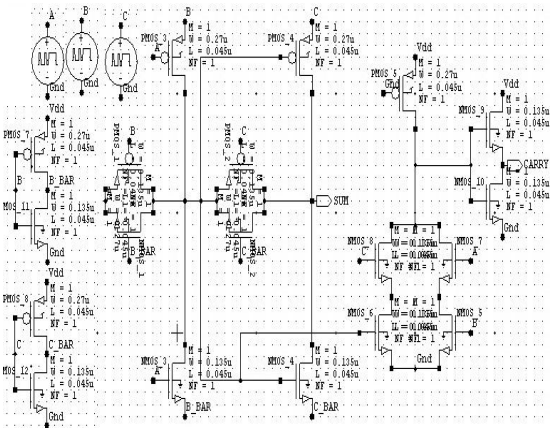

Fig.7.Circuit Diagram of TG Pseudo Full Adder

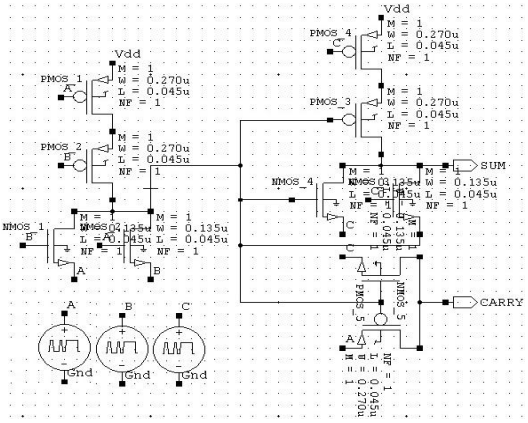

Fig.8. Circuit Diagram of SERF Adder Circuit

2.6 SERF Adder Circuit

SERF adder circuit is shown in Figure 8. 4 transistors are recognize in circuits be made up of two XNOR's. Output of the second stage of XNOR circuit has produced the sum. Carry can be intended by multiplexing A and C, and managed by (A ⊗ B). Our first XNOR module at output node is considered being a capacitor. We consider an example to illustrate the static energy recovery as A = B = 0 and then 1. Let A and B are both equal to zero when the capacitor is charged by $V_{DD}$. B in the next step, while keeping a high voltage level reaches a low voltage to a fixed level, the capacitor discharges through. Some charges are retained. After achieving high voltage stage, capacitor does not fully charge. As a result, power is less utilized.

2.7 14T AND 16T Full Adder Circuits

Fourteen transistors (14T) and sixteen transistors (16T) are elevated the performance of full adder is revealed in the circuit diagrams by low power XOR-XNOR (4T) and Transmission gates combination. A non-full swing is generated by pass-transistors arrangement.14T full adders are shown in Figure.9 and Figure.10. This circuit operate the low power XOR/XNOR circuit to drive the transistor network [38] also generate a full swing carry signal using four transistors which do not afford sufficient dynamic power . Losses due to threshold voltage and with the effect of low- power and low- voltage applications are incompatible for this circuit at node Y and also for non -zero standby energy utilization .

16T full adder, as shown in Figure.11 and Figure.12. DCVS circuit has derived from full swing generating signal XOR and XNOR circuit by using a pass transistor. In internal nodes, it has a difficulty of threshold losses related to 14 Transistors, but loss is not transmitted to output node.

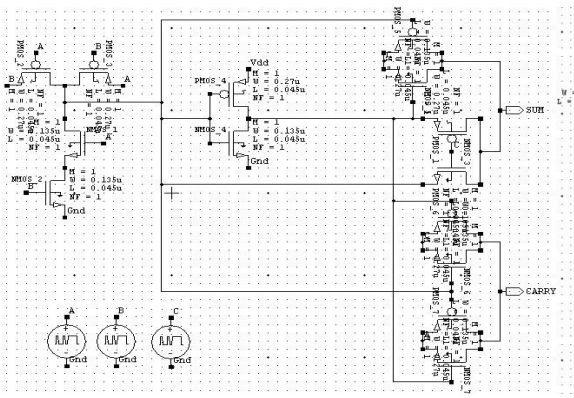

Fig.9. Circuit Diagram of 14T (Cascade Output)

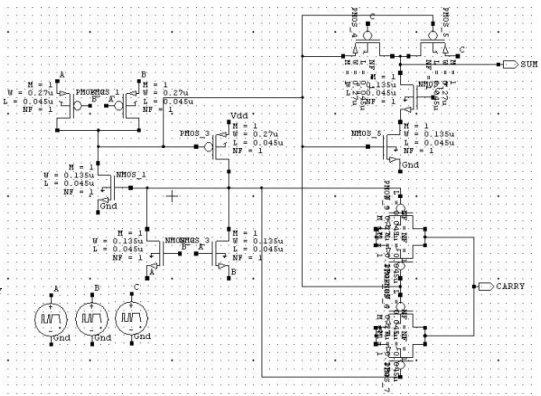

Fig.10. Circuit Diagram of 14T (Centralized Output)

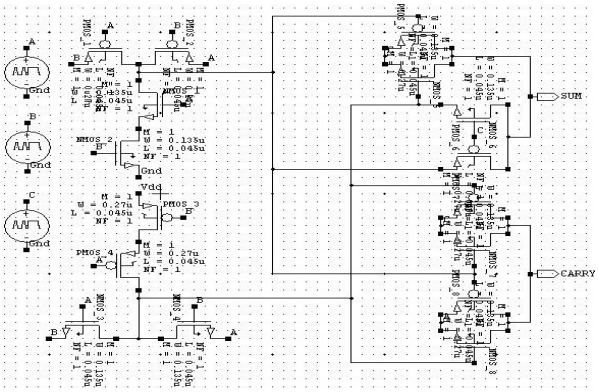


Fig. 11.Circuit Diagram of 16T (Cascade Output)

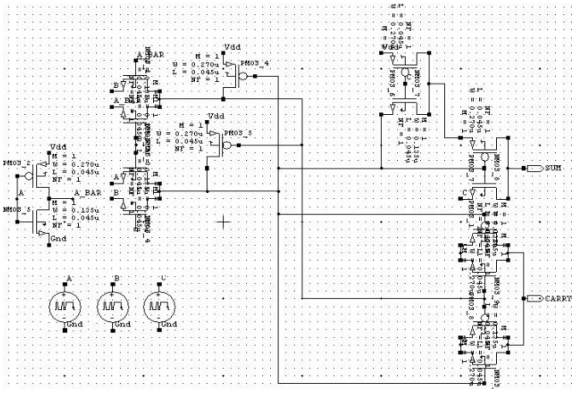


Fig.12. Circuit Diagram of 16T (Centralized Output)

2.8 Gate Diffusion Input (GDI) Full Adder

XOR and XNOR gates, these two different GDI full adders -based structure were intended. GDI -based full adders of the circuit operation is related to the previous SERF section. Sum bit XOR is achieved from the output of the second phase of XOR and XNOR shown in Figure.13 and Figure.14 respectively. Carry bit is designed by the controlling (A XNOR B) and multiplexing B and C the circuits. Advantage of the design is that GDI cell functionally flexible than the CMOS design due to two additional input pin applied. It is also an intellect propose with very energy efficient, without a enormous quantity of transistor count.

The main difficulty is to understand a GDI cell which is involved on twin- well CMOS or silicon insulator (SOI), develop to recognize. Therefore, it would be more costly to a GDI chip. If we are applied a model of P-Well CMOS GDI project will face the difficulty of driving capability. As a result, it may more costly as well as not easy to recognize like a practical chip.

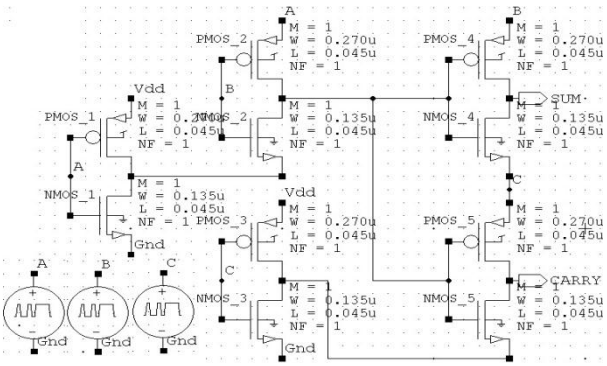


Fig.13.Circuit Diagram of GDI XOR

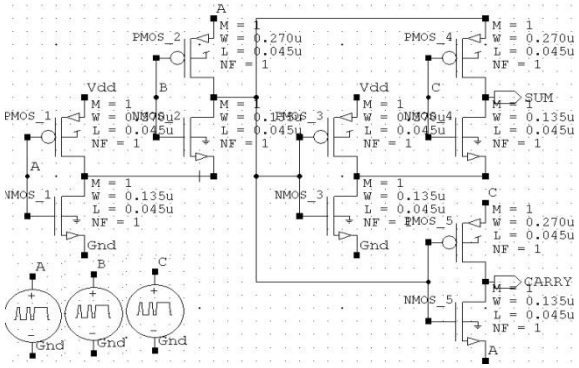


Fig.14. Circuit Diagram of GDI XNOR

2.9 Multiplexer Based Full Adder Circuits

In these full adder circuits 12 transistors is being employed. This is based on full- adder cell, which has been put into operation in six multiplexers. Pass transistor logic is applied to construct of each multiplexer. This circuit has neither $V_{DD}$ nor ground signal, that's why the power consumption has been reduced drastically. In the figure, we have noticed that there are several paths including a three series of transistors. It shows an enhancement in delay production of sum signal. Descriptions of 12T Body - Boot – buffer are taken out from literature [8]. For decreasing power indulgence, the threshold voltage is raised. It is guaranteed that the value for ground is reserved to negative and positive for power. Production of carry, transmission gate is required. Even though advantages are to get better region, the speed and power utilization, it is desirable that noise is built up due to addition of an inverter to the output.

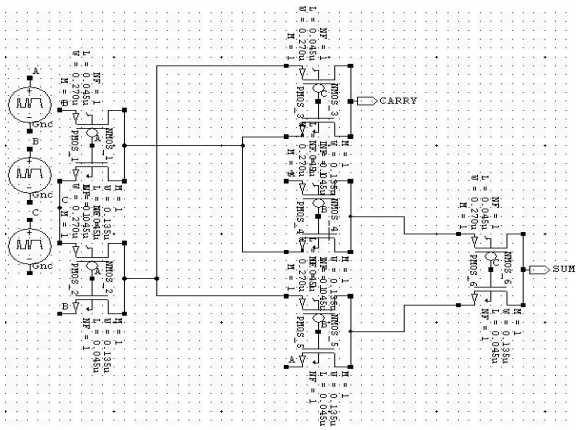


Fig. 15. Circuit Diagram of MUX Based Full Adder

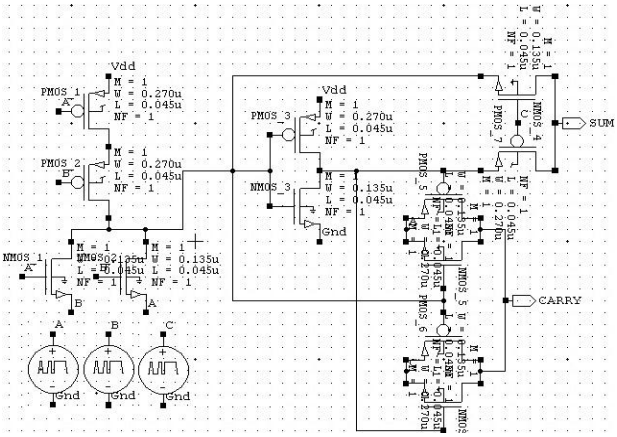


Fig. 16. Circuit Diagram of 12T Body- Bootstrapped

2.10 10T (4T) Full Adder Topologies

The basic benefit of 10T full adders is minor region and minimum power utilization. A few of the 10T full adder section is revealed in Figure.17 and Figure.18. The minimum propagation delay of circuits can be considered by swapping input. 10T adder cell is an optimal design of XOR function as well as realization of logic functions is being formed pass transistor logic. Function of two XOR required determining the sum operation. XOR operation for each four -transistor (4T) is mandatory. CARRY operation is to implement using two transistors with the help of 2:1 MUX. 9A full adder is shown in Figure 19 with 4T (XOR-XNOR) model and also groundless XNOR formation as well as 2:1 MUX. 9B full adder is shown in Figure 20 with 4T (XOR-XNOR) model and also groundless XNOR formation as well as 2:1 MUX. 9B Full Adder can be originated from 9A full adder by swapping the input of four-transistor groundless XNOR.

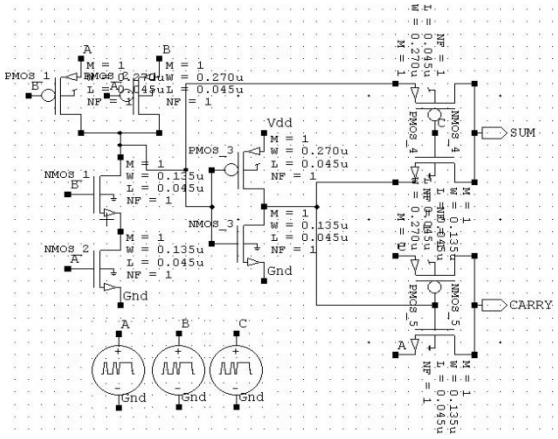


Fig.17. Circuit Diagram of 10A (4T) Adder

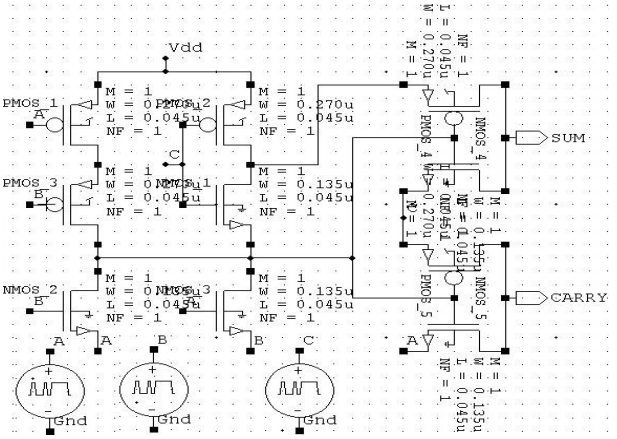


Fig.18. Circuit Diagram of 10B (4T) Adder

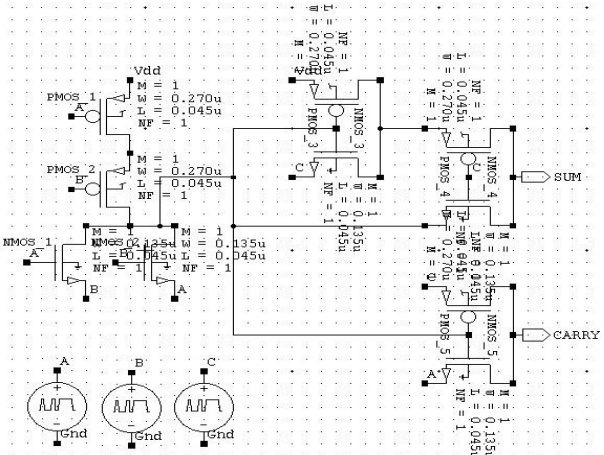


Fig.19. Circuit Diagram of 9A (4T) Adder

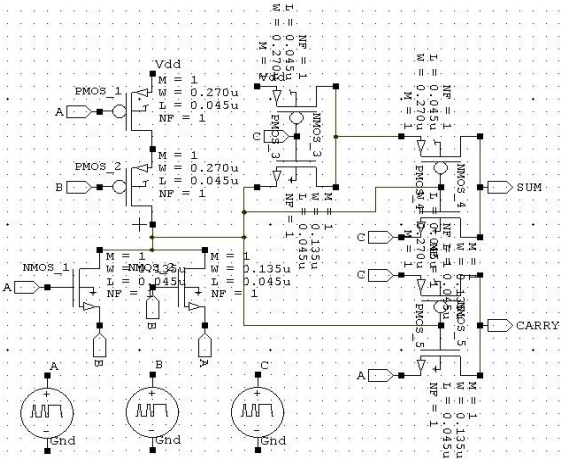


Fig.20. Circuit Diagram of 9B (4T) Adder

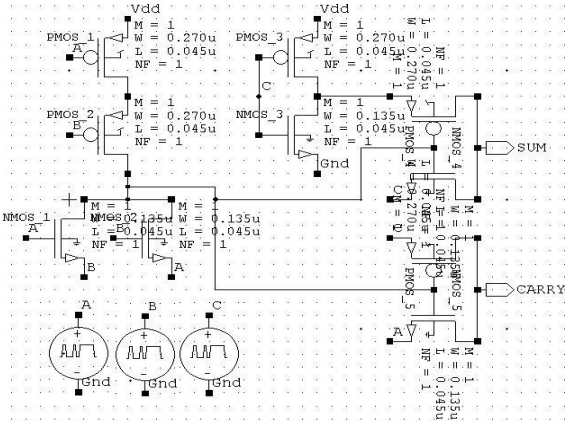


Fig.21. Circuit Diagram of 13A Adder

2.11 CLRCL Full Adder Circuits

Complementary and Level Restoring Carry Logic (CLRCL) adder [12] reported that it may minimize the damage of threshold of a 10T adder. Figure.22 shows the circuit diagram of CLRCL Adder in the connection of CLRCL, 2:1 MUX and the CMOS inverters produce the Sum and Carry functions using the subsequent Boolean equations:

$$Sum = (A \oplus C).\overline{Carry} + \overline{(A \oplus C)}.B \tag{8}$$

$$Carry = (A \oplus C).B + \overline{(A \oplus C)}.A \tag{9}$$

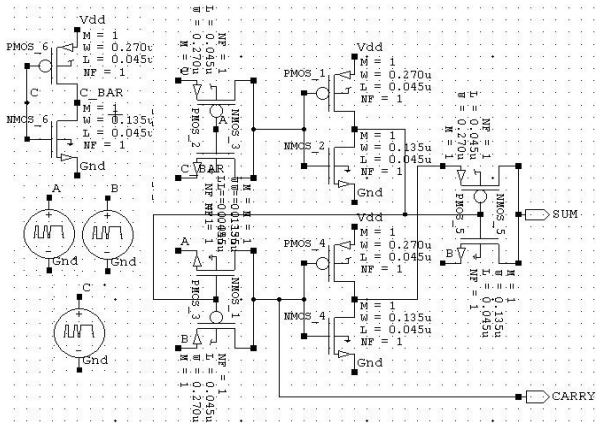


Fig.22. Circuit Diagram of CLRCL Full Adder

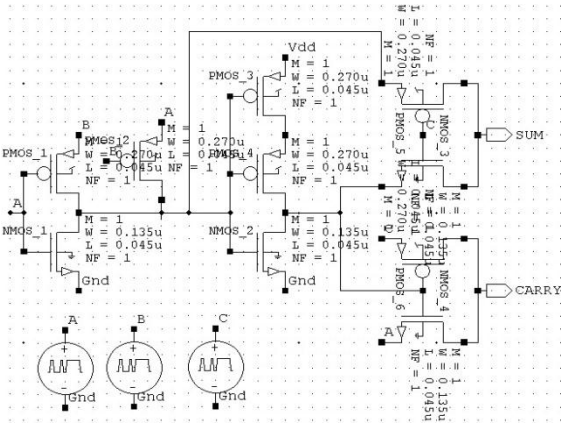


Fig.23. Circuit Diagram of 10T (3T) Full Adder

2.12 10T (3T) Full Adder

Depending on nationalized structure 10T (3T) full adder is shown above in Figure 23. In-between XOR and XNOR logic three transistor (3T) XOR and XNOR gate [34] is used to produce Sum and carry using two-transistor multiplexers. Owing to short circuit current in ratio logic, XOR and XNOR (3T) devour high energy. Basic benefits of 10T transistor full adder are smaller amount of area, higher gate count, less power utilization and less operating voltage. It is pursued by a less transistor count; full voltage swing operation is very complicated and less power consumption.

2.13 9T (3T) Full Adder

In nine transistor (9T) full adder module, there have only one XOR (3T) gate, as revealed in the Figure. 24, Figure.25 and Figure.26 [17-21] respectively. 3T XOR circuit is intending with the help of CMOS inverter and a PMOS pass transistor. If input B is at logic high, it performs like CMOS inverter. But when input B is at a logic low, CMOS inverter output is in high impedance. However , the pass transistor M3 is activated and the output Y obtain the similar logic value like input A. Decreasing in voltage, because of threshold drop arise transversely into pass transistor when A=1 and B=0 and the output Y is dishonored with regard to the input .

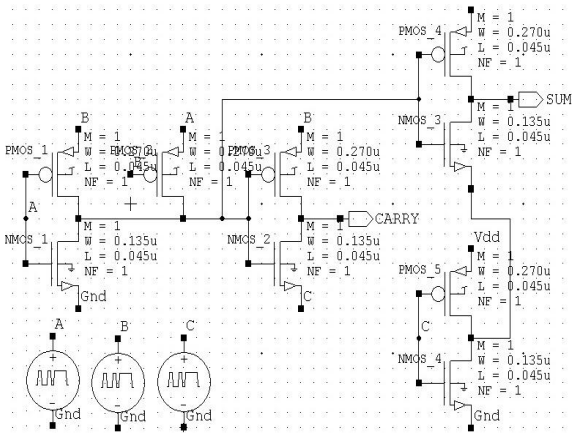


Fig.24.Circuit Diagram of 9T (3T) Full Adder

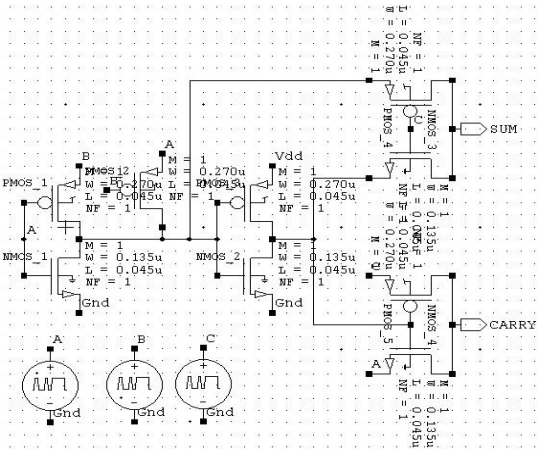


Fig.25. Circuit Diagram of 9T (3T) Full Adder 1

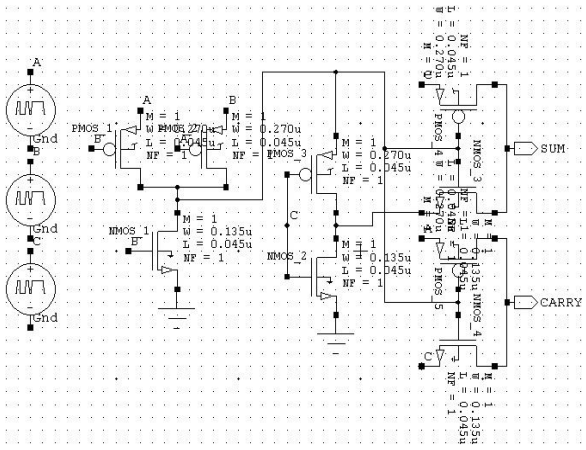


Fig.26. Circuit Diagram of 9T (3T) Full Adder 2

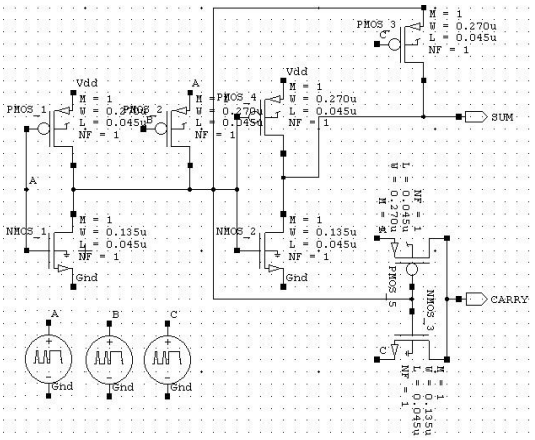


Fig.27. Circuit Diagram of 8T (3T) Full Adder

2.14. 8T (3T) Full Adder

Deriving from XOR (3T) function, an eight- transistor (8T) full adder proposal is shown in Figure 27. 8T full adder has three sections - two XOR (3T) gates and a multiplexer (2T) exists. Due to the least amount of transistors, this delay may be derived at high speed with low power dissipation. Eight- transistor (8T) is another blueprint of an eight transistor (8T) equation which is derived from Boolean XOR (3T) gates.

$$\text{Sum} = A \oplus B \oplus C \text{ and Carry} = C.(A \oplus B)+A.B \quad (10)$$

The sum output is achieved by a cascading XOR (3T) gates. Carry function is able to be comprehend by a wired OR logic in agreement with the above equation. The Layout of 8T Full Adder is shown in Figure.28.

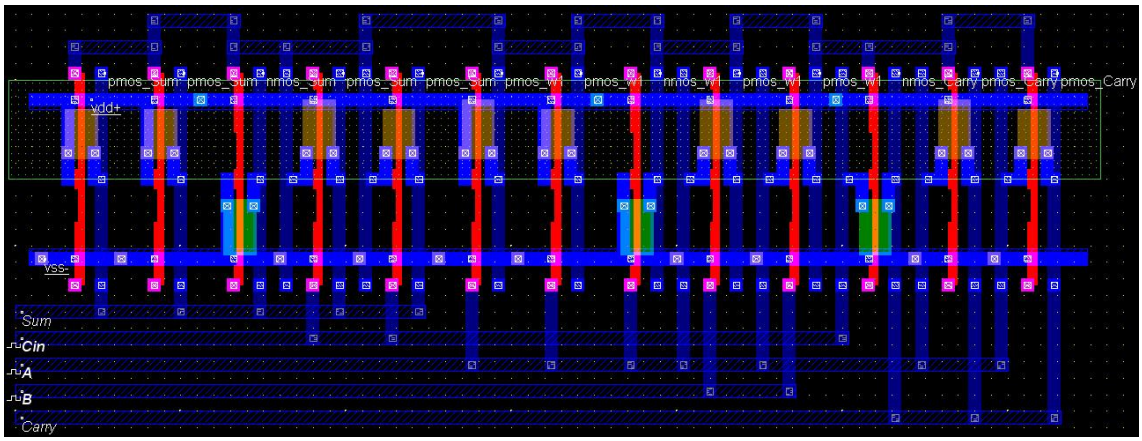


Fig.28. Layout of 8T (3T) Full Adder

## III. Result Analysis

All the circuits have been simulated in Tanner Spice-13 in 45nm Technology. The Layout has been generated in Microwind2. The input voltage is taken as 0.5V. The frequency of operation is taken as 1000MHz. The comparison of Transistor Count has been given in Fig.29. The Noise, Power, Delay, Area of all the circuits has been given in Fig.30, Fig.31, Fig.32, Fig.33 respectively.

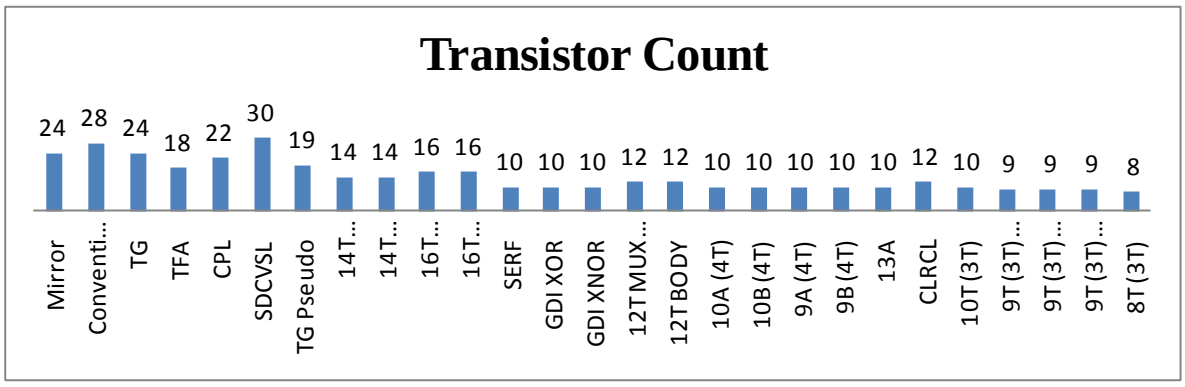


Fig.29. Comparison of Transistor Count of different Full Adder Circuit

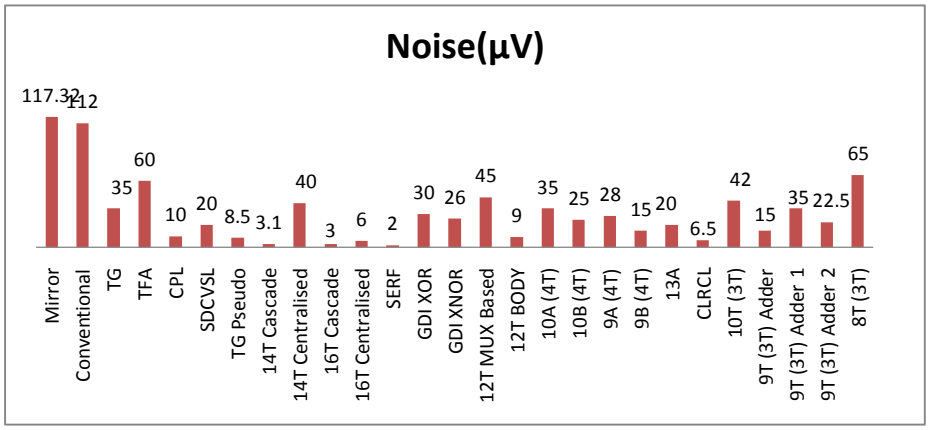


Fig.30. Comparison of output Noise of different Full Adder Circuit

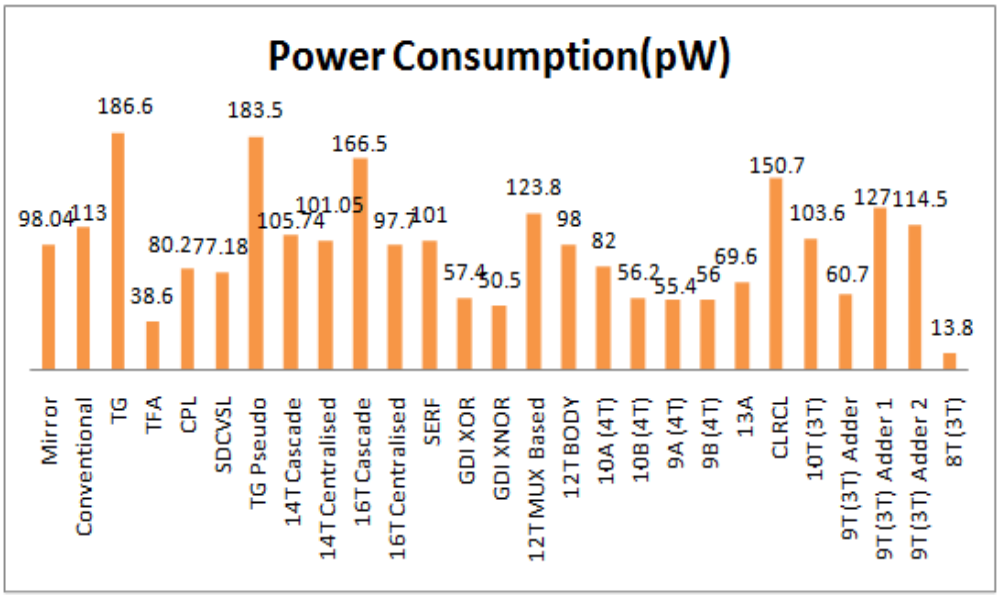


Fig.31. Comparison of Average Power Consumption of different Full Adder Circuit

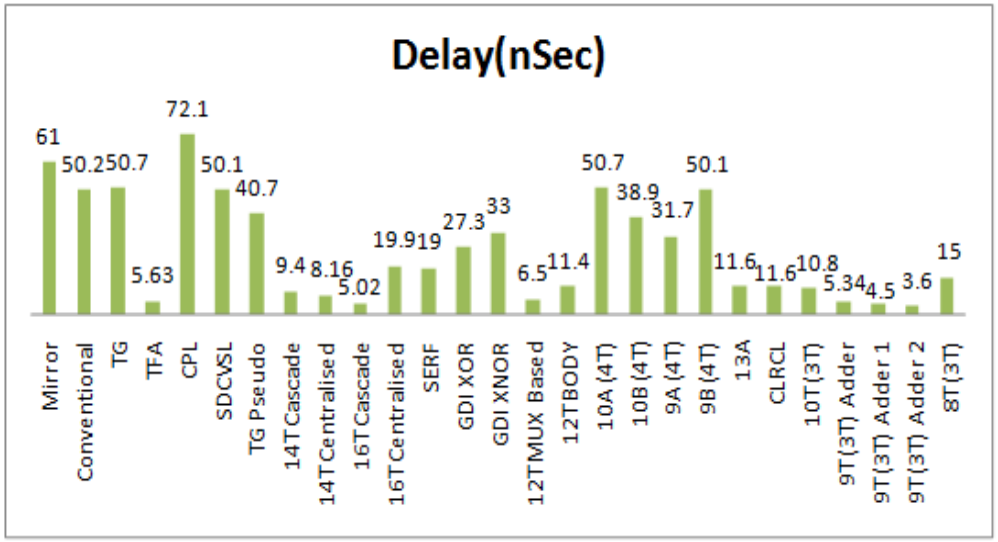


Fig.32. Comparison of Delay of different Full Adder Circuit

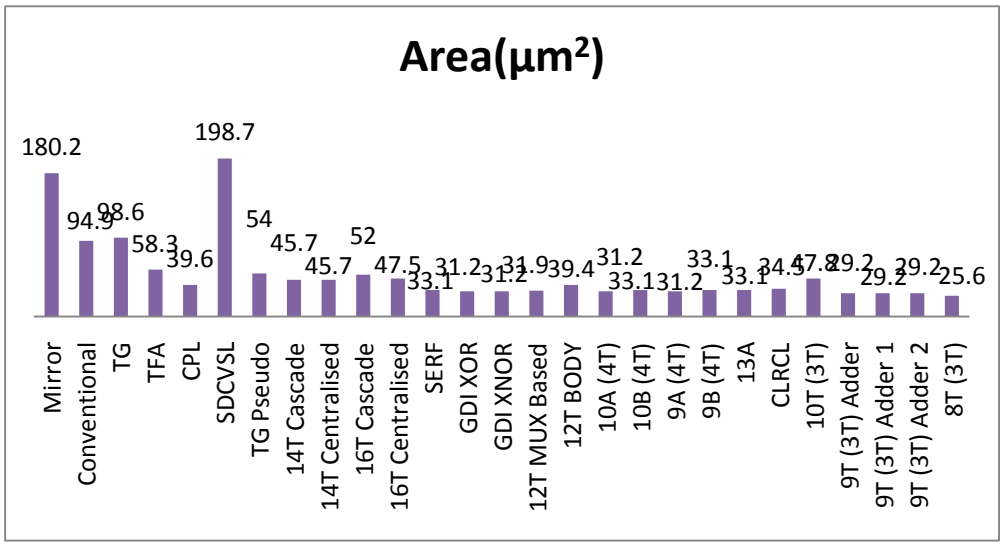


Fig.33. Comparison of Area of different Full Adder Circuit

## IV. Conclusion

In this paper, the common kinds of adders have been considered in terms of power, low-level design flow hypothesis, which is quite monotonous. But present design flows offer the most precise results, or a high-level design flow hypothesis, which is normally used. The various adder designs are derived by merging XOR (XNOR) (4T/3T) gates. The newly implemented 8T adder circuit discussed in this study is superior application to high performance multipliers with low power consumption. The latest design full adder can offer full voltage swing at a low supply voltage and suggest better performance in respect of power, delay, and noise as compared to the conventional full adders. Different arrangements of XOR function and TG with PT (powerless/groundless) circuit have been executed, simulated, analyzed and compared. Based on our extensive simulations, the 8T adder consume significantly less power in the order of Pico watts and having higher speed and consumes lesser area compare to the other designs of full adder circuits under different simulation parameters.

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